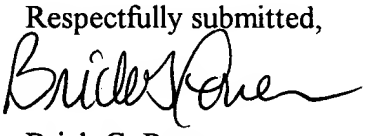
REMARKS

No new matter has been added. The Applicants again request entry of the amendments as set forth in the Appendices hereto prior to examination of the application on the merits.

Respectfully submitted,



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BGP/df/blh

VERSION OF SPECIFICATION WITH MARKINGS TO SHOW CHANGES MADE

Please replace paragraph **[0003]** with the following:

[0003] Background of Related Art: Conventionally, spin-on processes have been used to apply substantially planar layers of material to the surfaces of semiconductor device structures being fabricated upon a wafer of semiconductor material (e.g., a silicon, gallium arsenide, or indium phosphide wafer) or other semiconductor substrate (e.g., a silicon on insulator (SOI), silicon on glass (SOG), silicon on ceramic (SOC), silicon on sapphire (SOS), or other similar substrate). Consequently, while the portions of a spun-on layer of material over substantially horizontal structures may be substantially planar, the layer of material may not substantially fill or conform to the numerous, minute recesses formed in the semiconductor device structure.

Please replace paragraph **[0042]** with the following:

[0042] Referring now to FIG. 3, once a mask layer 18 with a substantially planar surface 19 is formed, the portions of mask layer 18 and of hemispherical grain silicon layer 16 that are located above a plane of surface 12 are removed from stacked capacitor structure 10. In order to reduce or eliminate the creation of potentially contaminating debris and of surface defects that may be caused by mechanical planarization processes, layers 18 and 16 are removed by known chemical processes, such as dry etch processes or wet etch, or wet dip, processes. For example, mask layer 18 may be selectively removed by use of a known resist strip, then layer 16 removed from surface 12 with a wet etchant that removes silicon with selectivity over the portions of mask layer 18 remaining in containers 14 and over an underlying dielectric layer 15. As another example, layers 18 and 16 may be substantially concurrently removed with an etchant or combination of etchants that will remove mask layer 18 and hemispherical grain silicon layer 16 at substantially the same rates. Mask material remaining in containers 14 may then be removed by known processes, such as the use of known wet or dry strip materials (e.g., an ammonium hydroxide (NH_4OH) dry strip known in the art as a "piranha" strip when the mask material is ARCH 895 or a similar photoresist). This process provides a stacked capacitor structure 10 with conductively doped hemispherical grain silicon 16-lined containers 14 recessed in a substantially[-]_defect and contaminant-free surface 12 of structure 10 and dielectric layer 15, as shown in FIG. 4. Stacked capacitor structure 10 shown in FIG. 4 may then be processed as known in the art to fabricate a finished stacked capacitor.

Please replace paragraph **[0050]** with the following:

[0050] Alternatively, once a substantially planar surface 31 has been formed over shallow trench isolation structure 30, as shown in FIG. 9, stress buffer layer 38′ and the portions of insulator layer 36 located above the plane of surface 22 may be substantially concurrently removed from above shallow trench isolation structure 30 by use of one or more dry or wet etchants that remove the materials of layers [38] 38′ and 36 at substantially the same rates, as known in the art, or by known chemical-mechanical planarization processes to provide the finished shallow trench isolation structure 30 illustrated in FIG. 11.

Please replace paragraph **[0052]** with the following:

[0052] FIGs. 12-16 illustrate yet another embodiment of a semiconductor device structure 40 that incorporates teachings of the present invention. With reference to FIGs. 12 and 13, semiconductor device structure 40 includes dual damascene trenches 44 formed in a surface 42 of an insulator layer 41 thereof. A conductive layer 46 overlies surface 42 and substantially fills trenches 44. Conductive layer 46 has a nonplanar upper surface 47 that includes valleys 54 located substantially over trenches 44 and peaks 52 located substantially over surface 42. Insulator layer 41, trenches 44, and conductive layer 46, as well as other structures of semiconductor device structure 40 underlying insulator layer 41 and trenches 44 are each fabricated by known processes, such as those disclosed in U.S. Patent 5,980,657 to Farrar et al. issued on November 9, 1999, the disclosure of which is hereby incorporated in its entirety by this reference.

Please replace paragraph **[0054]** with the following:

[0054] Once a substantially planar surface is formed over semiconductor device structure 40, such as that formed at least partially by surface 49 of stress buffer layer 48 and as illustrated in FIG. 12, stress buffer layer 48 and portions of conductive layer 46 located above the plane of surface 42 may be substantially concurrently removed. For example, layers 48 and 46 may be substantially concurrently removed with an etchant or combination of etchants that will remove stress buffer layer 48 and [insulator] conductive layer 46 at substantially the same rates to provide the finished semiconductor device structure 40 illustrated in FIG. 16. Either wet etchants or dry etchants may be used. Preferably, the use of etchants eliminates the formation of imperfections or defects in surface 42 of insulator layer 41, as well as the possible introduction of contaminants or other debris thereon. Alternatively, known chemical-mechanical planarization

processes may be used to substantially concurrently remove stress buffer layer 48 and portions of conductive layer 46 above surface 42, also providing a finished semiconductor device structure 40 such as that illustrated in FIG. 16. As stress buffer layer 48 provides a substantially planar surface over [shallow trench isolation] semiconductor device structure 40, the likelihood that material of conductive layer 46 will be broken off during the chemical-mechanical planarization process is reduced, thereby reducing the formation of imperfections or defects in surface 42, as well as the creation of contaminants or other debris, which may occur during chemical-mechanical planarization of a nonplanar surface.

VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

4. (Amended) The semiconductor device structure of claim 3, further comprising at least one conductively doped region continuous with a surface of said semiconductor substrate and laterally adjacent said at least one [trench] recess.

5. (Amended) The semiconductor device structure of claim 1, wherein said substrate comprises:

a shallow trench isolation structure including a semiconductor device substrate with a surface and at least one trench formed in said surface of said semiconductor device substrate; and

an insulator layer substantially filling said at least one trench and covering said surface of said semiconductor device substrate.

17. (Amended) The semiconductor device structure of claim 15, further comprising:

at least one intermediate layer between said substrate and said material layer, at least one portion of said at least one intermediate layer at least partially filling said at least one recess.